

[www.chip2foil.eu](http://www.chip2foil.eu)  
[m.tichem@tudelft.nl](mailto:m.tichem@tudelft.nl)

Marcel Tichem, Scientific coordinator  
TU Delft, Micro and Nano Engineering Laboratory  
OLAE Cluster Concertation Meeting  
Brussels, June 14-15, 2010

# Chip2Foil in a nutshell

- Chip2Foil main aim: *to develop a technology platform for high speed, low cost placement and interconnection of ultra thin chips on thin polymer foils*
- EU FP7 STREP
- Call ICT-2009.3.3 – Flexible, organic and large area electronics
- Started Jan 1, 2010; duration 3 years
- ~M€4.7 project size, ~M€2.9 EU contribution
- 7 partners: TU Delft (NL), Holst Centre (NL), IMEC (B), DSM (NL), Orbotech (ISR), Datacon (A), Plastic Electronic (A)



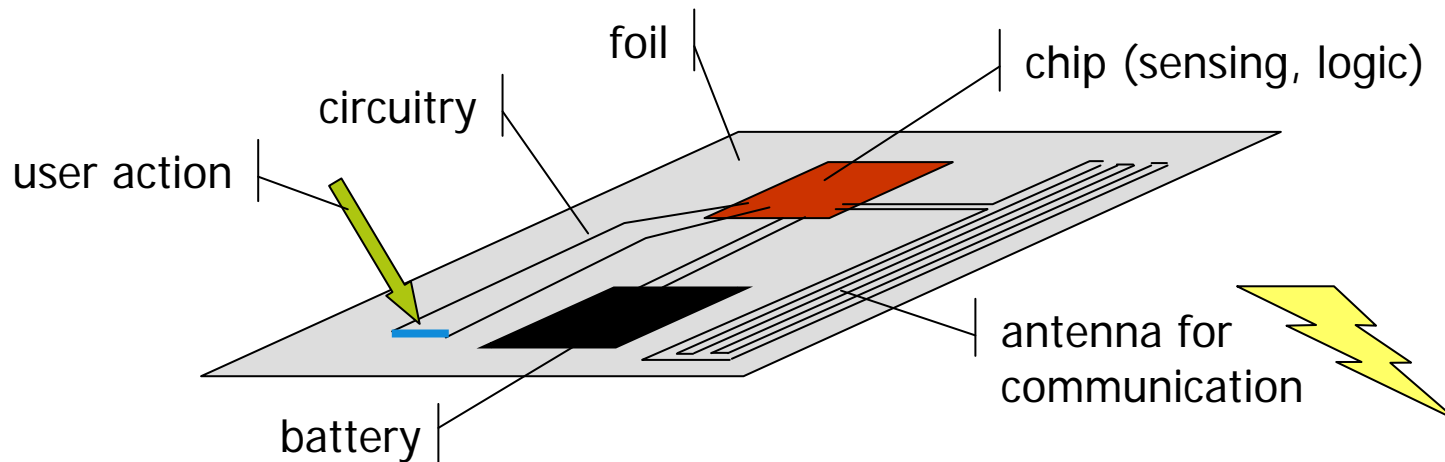
# Communicative foil-based packages



Smart Blister

Food labels

# Functions communicative foils

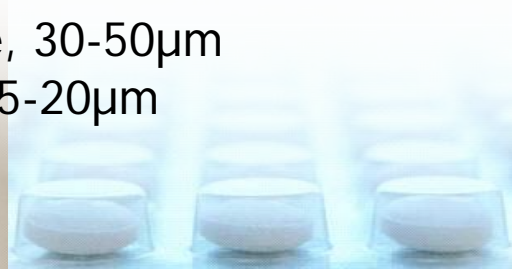


- Focus of Chip2Foil: ultra thin chip integration
- Total process flow: from processed wafer to bonded and interconnected chip
- Demonstrate process flow by realising SmartBlister device

# Demands

## Flexible package

- Foil-based thin package, 30-50 $\mu$ m
- Ultra thin chip (UTC), 15-20 $\mu$ m



## Low cost

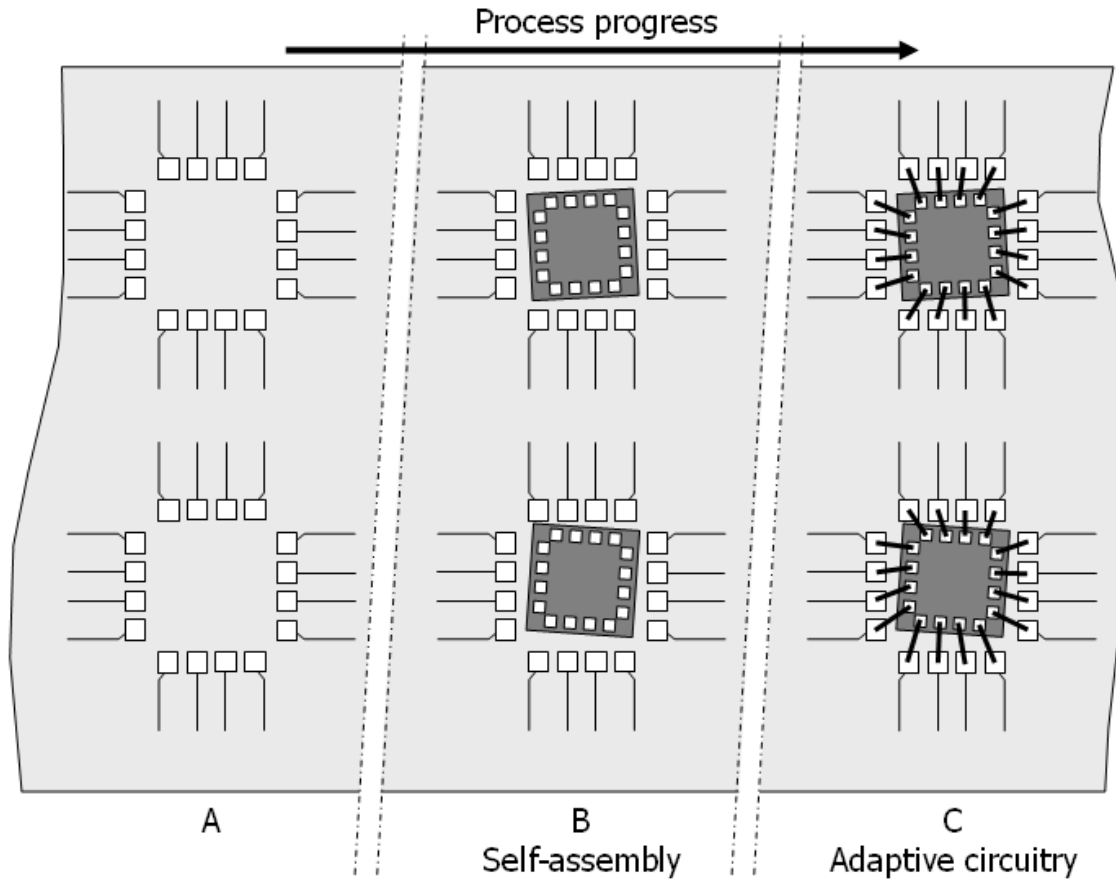
- Single foil
- PEN or PET
- Single chip, 1x1mm<sup>2</sup>

## Advanced RFID chips

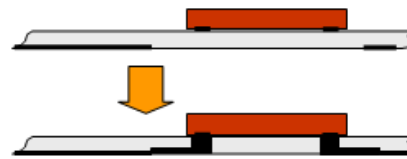
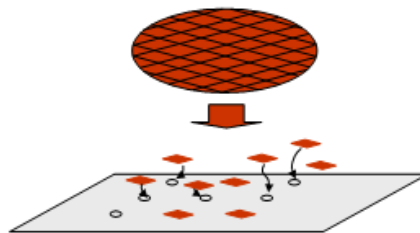
- 20-40IO
- Clock function

## High volume

- Billions of packages/yr, 10-50 chips/s
- Reel-to-reel compatible



- **Self-assembly:**  
high throughput and low cost, moderate precision
- **Adaptive circuitry:**  
flexible low-cost interconnection



# Chip-placement

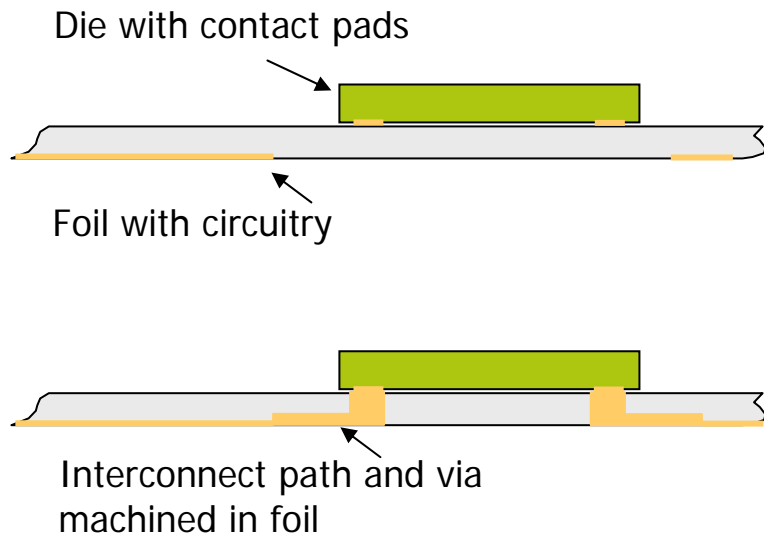
- Chip release and presentation – *speed up for ultra thin chips*
- Self-assembly – *high throughput, low cost, moderate accuracy*
- Mechanical bonding – *underfill, overcoat*

Self-assembly = autonomous assembly  
Physical principle to be selected

Magnetisable material on chip  
Trapping range ~1-2 chip size  
Alignment precision ~40-60 $\mu$ m (x,y)  
Speed: less than 0.5 second/chip

# Adaptive circuitry

- Various techniques for interconnect writing will be explored
- Laser-based machining





# Status

- Device specifications finished (June 2010)
- Technological options identified for all processes
  - Chip release and presentation
  - Self-assembly
  - Mechanical bonding
  - Electrical interconnection
- Research on individual technologies started
- Selection of feasible combination of technology options expected  
Dec 2010-June 2011



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