Ultra thin chip integration process for low cost communicative polymer foils CHIP2FOIL

Public Summary Year 1

Lead partner: TU Delft (Coordinator)

Contact:
Dr. Marcel Tichem
Laboratory for Micro and Nano Engineering
Department of Precision and Microsystems Engineering
E: m.tichem@tudelft.nl

1 Publishable Summary

1.1 Introduction

Chip2Foil aims at realising a technology platform for low cost placement and interconnection of ultra thin chips on polymer foils, within a high volume, reel-to-reel production concept. This competence allows realising a broad variety of disposable communicative packages. These packages provide increased interaction between the packed product, the package and the user through near-field communication systems, allowing improved intelligent control of the logistic process of high volume applications like medicine and food. The chosen demonstrator is a Smart Blister package, which monitors the medicine taking behaviour of patients to ensure therapy compliance. Therapy non-compliance is a severe ethical and economic problem, leading to considerable numbers of casualties per year and high health care cost.

A breakthrough is needed to raise the throughput of ultra thin chip placement and interconnection while reducing the cost. The proposed Chip2Foil technical concept combines two main elements: (1) self-assembly for high speed chip placement with moderate accuracy, and (2) an adaptive circuitry approach, which compensates the initial placement errors and creates electrical interconnects after the chips have been placed.

The main targets Chip2Foil aims to achieve are:

- Package: low cost, flexible, thickness 30-50µm;
- Chip: thickness 15-20µm, 1x1mm, 20-40 IO;
- 10-50 chips placed per second, which dictates the speed for all processes (chip release and presentation, assembly, bonding, electrical interconnection);
- Chip assembly is done on the basis of self-assembly;
- Electrical interconnection is done on the basis of an adaptive interconnection approach;
- Developed processes must have the potential to be reel-to-reel implementable;
- Total cost for placement and interconnection for the thin chips focused on is aimed to be as low as for thick chips at first.

The consortium consists of 7 partners (4 industrial of which 1 global end-user, 2 research centres, 1 university) and are leading partners in the field of flexible electronics and chip integration: Delft University of Technology (The Netherlands, Coordinator), Holst Centre/TNO (The Netherlands), Orbotech (Israel), IMEC (Belgium), plastic electronic GmbH (Austria), DSM (The Netherlands), Datacon Technology GmbH (Austria).

The project is divided into 7 work packages, of which 5 are technical and 2 are dedicated to management and dissemination respectively. Two WPs focus on the key techniques to be developed: self-assembly supported chip placement and electrical interconnection by an adaptive approach. There is a separate WP for technology integration and evaluation, and one for realization of a demonstrator communicative package for the SmartBlister application.

The duration of the project is 36 months, the total cost is ~4.7M€, the EU contribution is ~3M€.

The website of the project is WWW.CHIP2FOIL.EU

1.2 Progress 2010 (Year 1)

The current reporting period covers the first year of the Chip2Foil project. Major attention was paid, in particular at the start of the project, to get all activities started. The major objectives were met in this period: all planned Tasks have become active and started to deliver, the planned Deliverables and Milestones were achieved.

Major technical results were achieved in the WPs 2, 3 and 4. Detailed specifications of the package as well as some details on the specifications for the process flow were laid down and intensively discussed (WP2). In the prime package layout focused on, the chip is attached to the foil with the active side and contacts facing away from the substrate material. The chip is bonded to the substrate and overcoated with a globtop. The interconnects are fabricated in and on top of this globtop material.

A detailed process flow for chip placement, which includes chip release and presentation, self-assembly and mechanical bonding, was delivered (WP3). Initial experiments on various tools for chip release led to the choice to work on a multi-stage ejection tool. As a second chip release approach, laser-based die transfer was identified; work on this approach will start in 2011 (Year 2 of the project). While the first ejection approach is quite readily integratable into existing machine platforms, there may be a limit in speed of ejection and cost per ejection not satisfying the Chip2Foil demands. Laser-based die transfer on the other hand is industrially less mature, but does promise intrinsically higher speeds of release and higher logistic integration levels with the total process.
The selected self-assembly principle uses magnetic fields to self-align a chip with respect to target positions on the foil. Both the chip and the foil must be provided with ferromagnetic structures, which act as magnetic flux guides. Shape anisotropy of these structures and matching size leads to a unique final position and orientation of the chip with respect to the foil, while the initial chip position can be relatively coarse. To mobilize the chip during alignment it is floating on a dispensed thin layer of die attach adhesive. After alignment, the adhesive is cured by UV. In this way mechanical bonding is highly integrated with the entire chip placement process.

For electrical interconnection, three main techniques are focused on (WP4):

(1) Laser Induced Forward Transfer (LIFT): material transfer from a source to target using a laser source;
(2) Laser structuring of a screen-printed patch: cover the chip and circuitry on the web with a conductive patch which is structured to make specific interconnects;
(3) Sputtering/Cu plating (back-up solution).

Initial results for each technique have become available. For via drilling through the globtop material, the work on laser source selection has started. The partners involved in this task each research the laser sources available at their own labs in a coherent activity. The adaptive circuitry approach requires that the position of each individual chip is measured with respect to the circuitry on the foil. Experiments have been done to identify the bottlenecks in image grabbing, pattern recognition and position computation, and to define a suitable vision system.