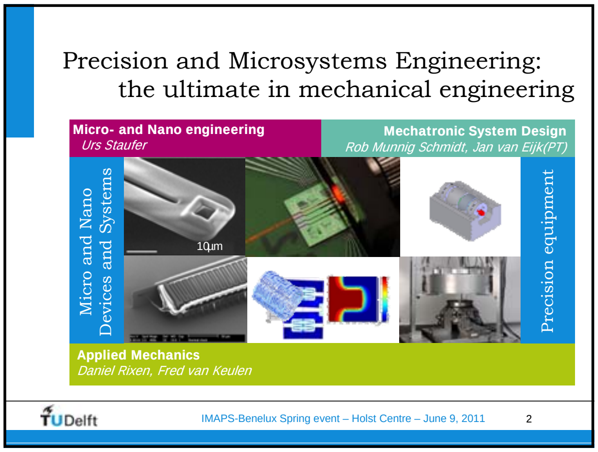
Harvesting the potential of self-assembly

Marcel Tichem, Delft University of Technology

IMAPS-Benelux Spring event, June 9, 2011 – Holst Centre

TU Delft Delft University of Technology

Challenge the future



Precision and Microsystems Engineering: the ultimate in mechanical engineering

Micro- and Nano engineering
Urs Staufer

Mechatronic System Design
Rob Munnig Schmidt, Jan van Eijk(PT)

Micro and Nano Devices and Systems

Precision equipment

Applied Mechanics
Daniel Rixen, Fred van Keulen

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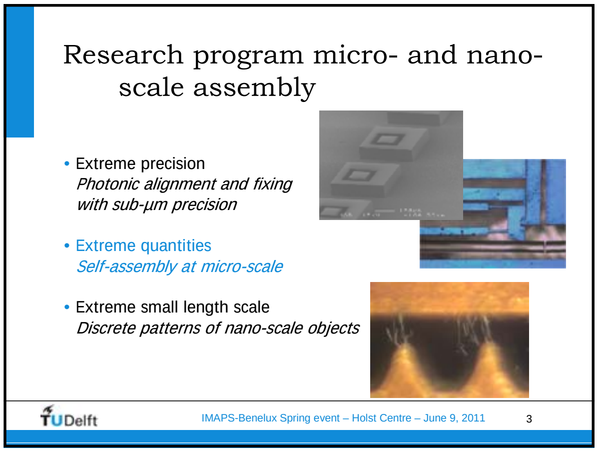

Research program micro- and nano-scale assembly

- Extreme precision
  Photonic alignment and fixing with sub-μm precision
- Extreme quantities
  Self-assembly at micro-scale
- Extreme small length scale
  Discrete patterns of nano-scale objects

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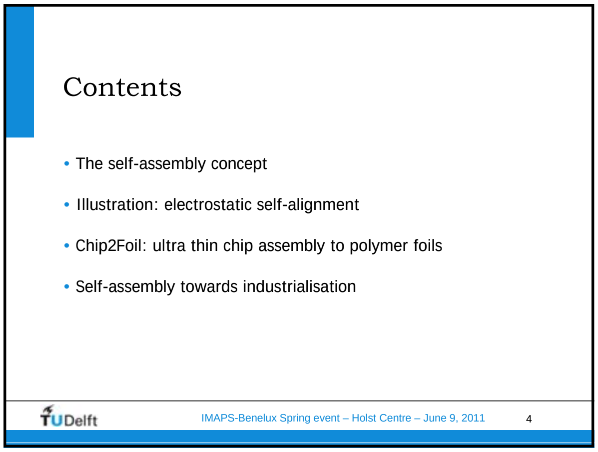

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- The self-assembly concept
- Illustration: electrostatic self-alignment
- Chip2Foil: ultra thin chip assembly to polymer foils
- Self-assembly towards industrialisation

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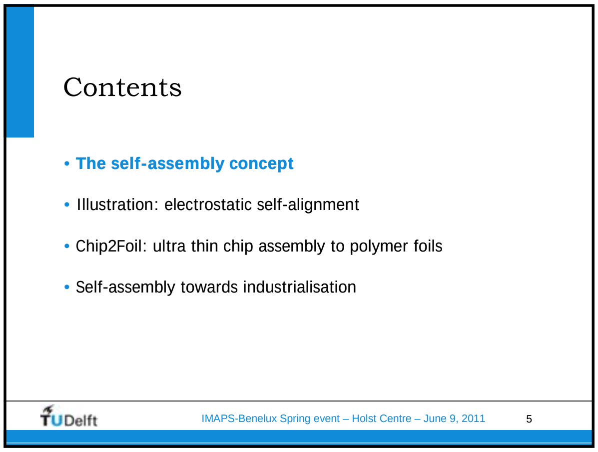

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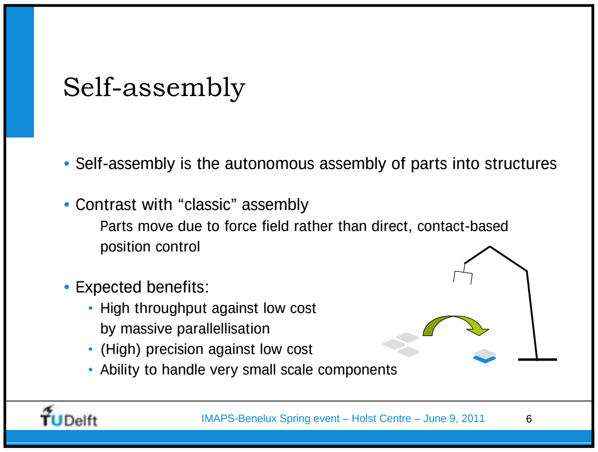

Self-assembly

- Self-assembly is the autonomous assembly of parts into structures
- Contrast with “classic” assembly
  Parts move due to force field rather than direct, contact-based position control
- Expected benefits:
  - High throughput against low cost by massive parallellisation
  - (High) precision against low cost
  - Ability to handle very small scale components

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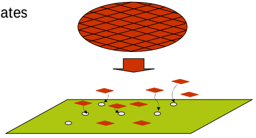
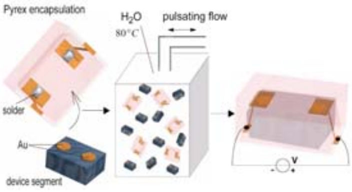
General self-assembly scheme

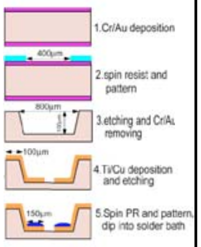
- At least one of the parts is put in random motion
  (usually – there is a form of self-assembly which uses hinging structures)
- Parts to be mated are provided with entrapment or binding sites, exploiting a force field which effectuates
  - Trapping
  - Alignment
  - Locking / bonding
- Various physical mechanisms may be exploited in the realisation of suitable binding sites



Self-assembly

Shape-and-solder directed self-assembly



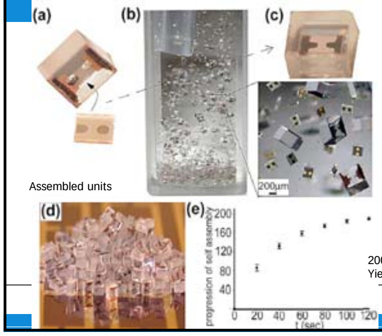


[Zheng04]

Processing of encapsulation units

Self-assembly

Shape-and-solder directed self-assembly



Assembled units

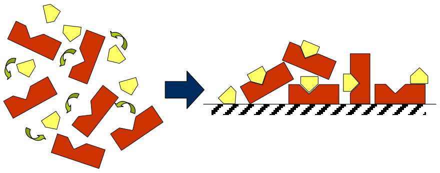
LEDs assembled manually on PCB and tested

Solder melting point 47°C
In water, temp 80°C
Component agitation by pulsating liquid flow

200 LEDs in 2 minutes
Yield 85%

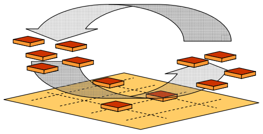
[Zheng04]

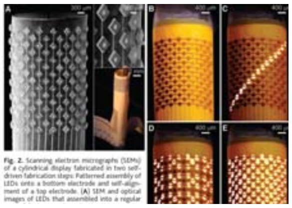
Logistic concept of this approach



- Efficient *sub*-operation
- Must fit in total process flow to harvest potential

Alternative main logistic approach and an implementation

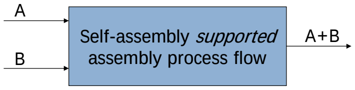




- "Flushing" parts over a surface with trapping sites

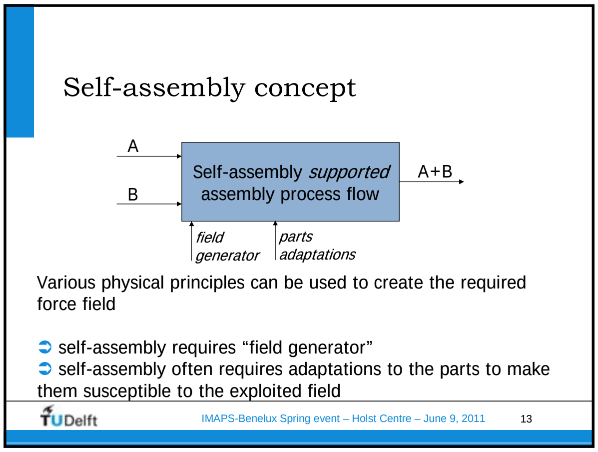
[Jacobs2002]

Self-assembly concept



Assembly = handling and joining
feeding, gripping, manipulating and placing, joining, adding substances, adjusting, …

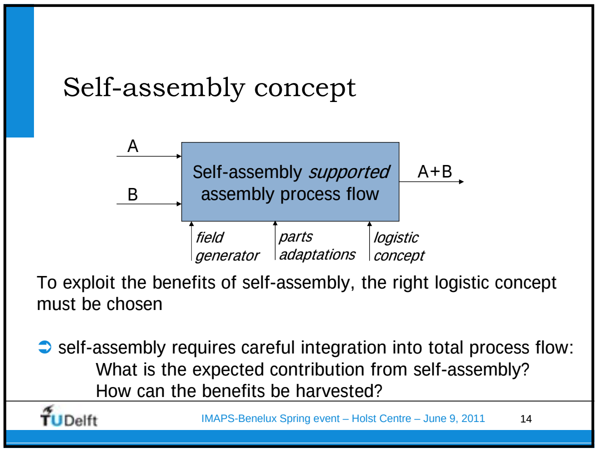
➲ self-assembly is about the part handling; sometimes bonding and/or electrical interconnection steps are integrated



Self-assembly concept

Various physical principles can be used to create the required force field

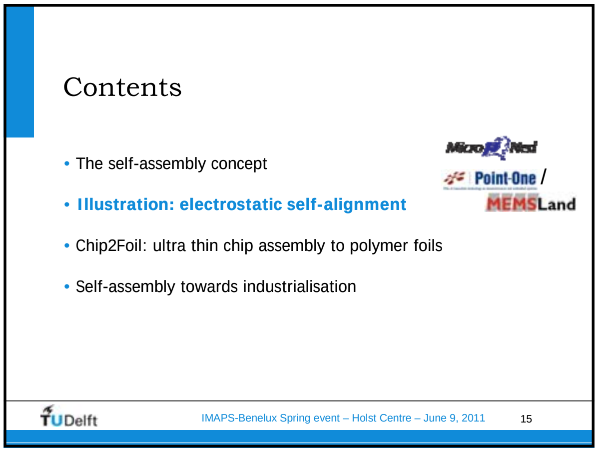
➲ self-assembly requires “field generator”
➲ self-assembly often requires adaptations to the parts to make them susceptible to the exploited field



Self-assembly concept

To exploit the benefits of self-assembly, the right logistic concept must be chosen

➲ self-assembly requires careful integration into total process flow:
What is the expected contribution from self-assembly?
How can the benefits be harvested?



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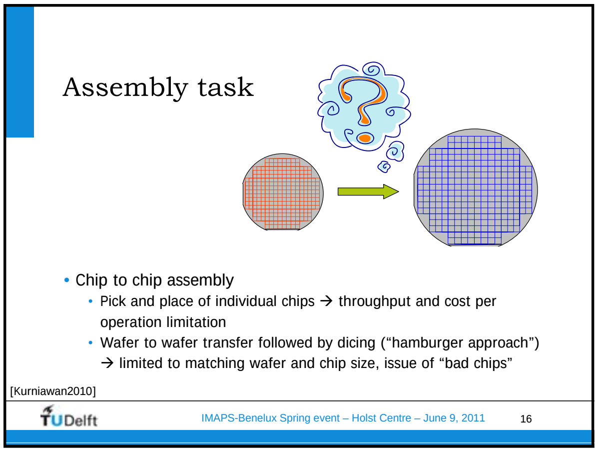
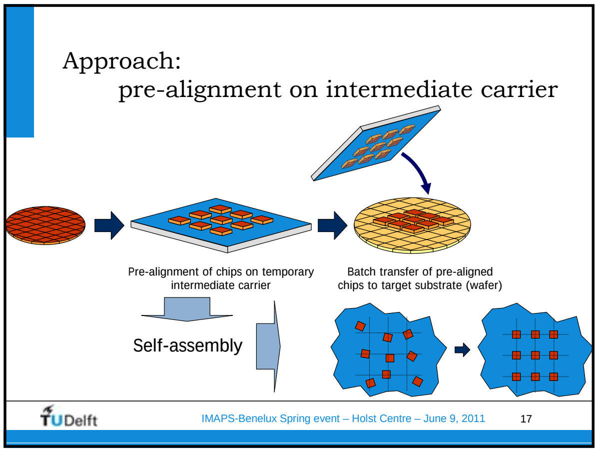


Assembly task

- Chip to chip assembly
  - Pick and place of individual chips → throughput and cost per operation limitation
  - Wafer to wafer transfer followed by dicing (“hamburger approach”) → limited to matching wafer and chip size, issue of “bad chips”

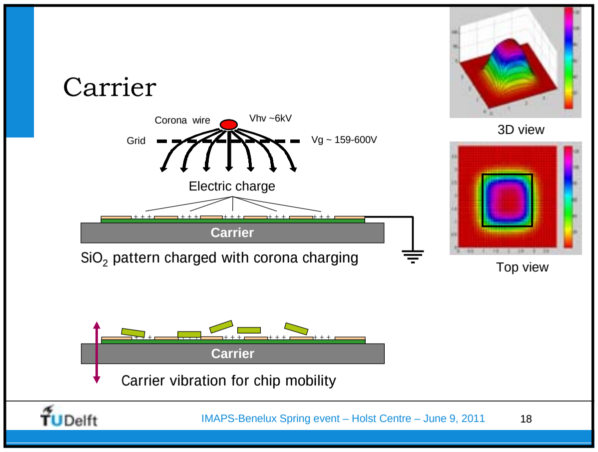
[Kurniawan2010]



Approach: pre-alignment on intermediate carrier

Pre-alignment of chips on temporary intermediate carrier

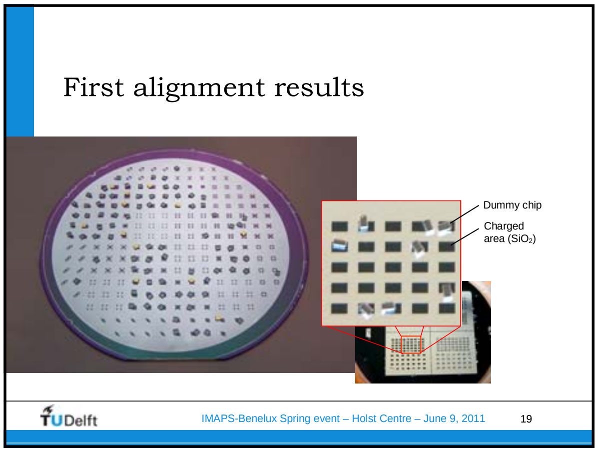
Batch transfer of pre-aligned chips to target substrate (wafer)



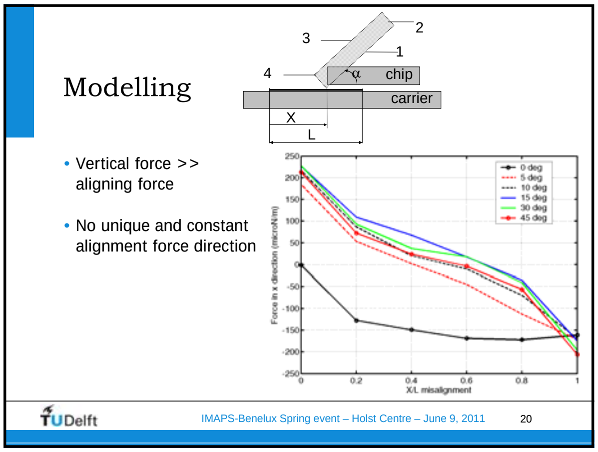
Carrier

SiO_2 pattern charged with corona charging

Carrier vibration for chip mobility

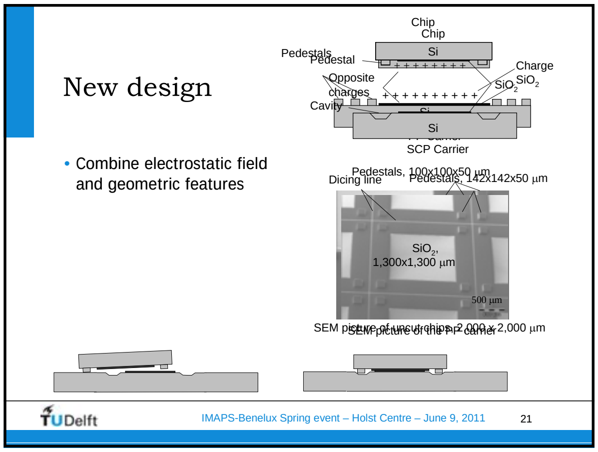


First alignment results



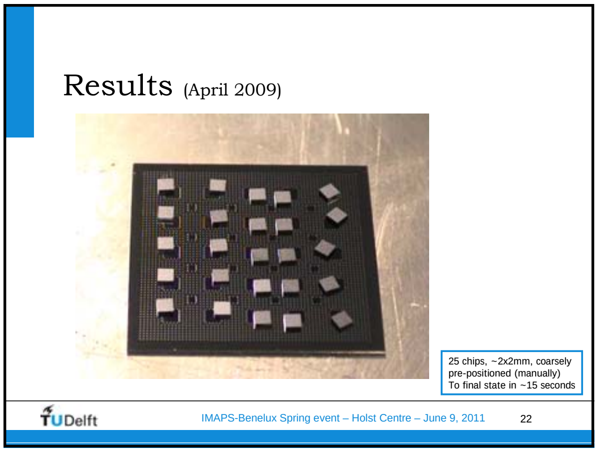
Modelling

- Vertical force >> aligning force
- No unique and constant alignment force direction



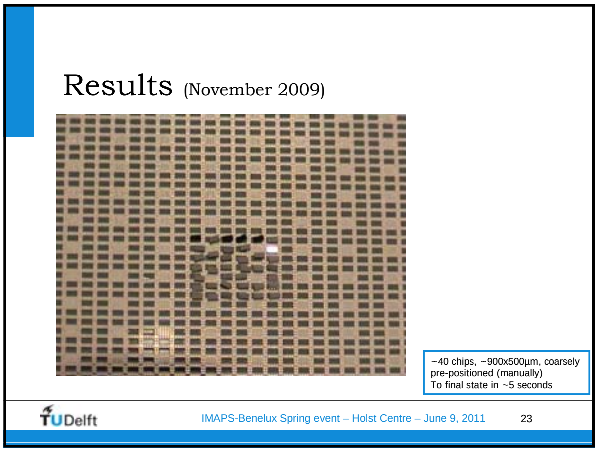
New design

- Combine electrostatic field and geometric features



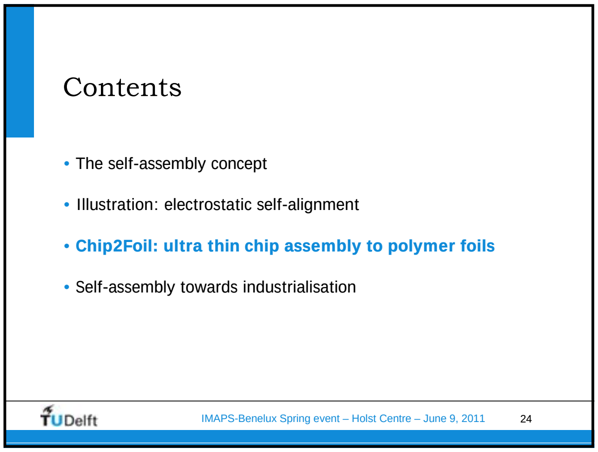
Results (April 2009)

25 chips, ~2x2mm, coarsely pre-positioned (manually)
To final state in ~15 seconds



Results (November 2009)

~40 chips, ~900x500μm, coarsely pre-positioned (manually)
To final state in ~5 seconds



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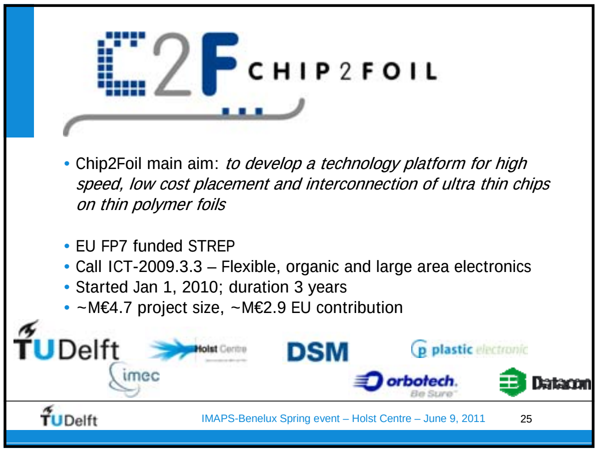


C2F CHIP2FOIL

- Chip2Foil main aim: *to develop a technology platform for high speed, low cost placement and interconnection of ultra thin chips on thin polymer foils*

- EU FP7 funded STREP
- Call ICT-2009.3.3 – Flexible, organic and large area electronics
- Started Jan 1, 2010; duration 3 years
- ~M€4.7 project size, ~M€2.9 EU contribution

Communicative foil-based packages

- Increased interaction packed product – package – environment

- Chip2Foil focused case: Smart Blister to ensure therapy compliance

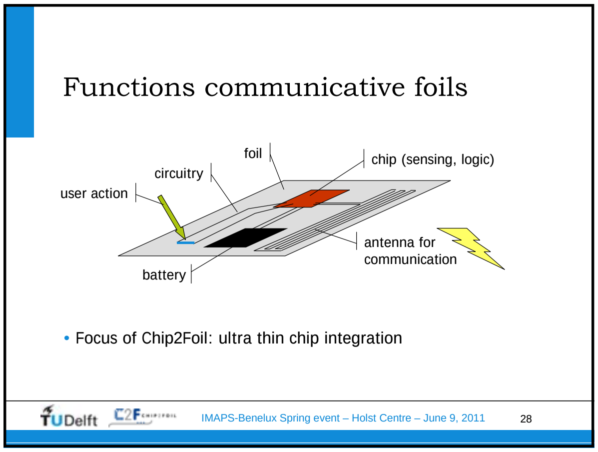
Demands

Flexible package
- Foil-based thin package, 30-50µm
- Ultra thin chip (UTC), 15-20µm

Low cost
- Single foil
- PET
- Single chip, 1x1mm^2

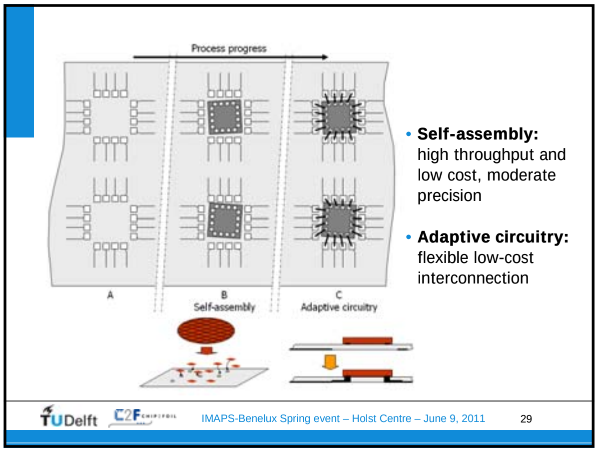
Advanced RFID chips
- 20-40IO
- Clock function

High volume
- Billions of packages/yr, 10-50 chips/s
- Reel-to-reel compatible



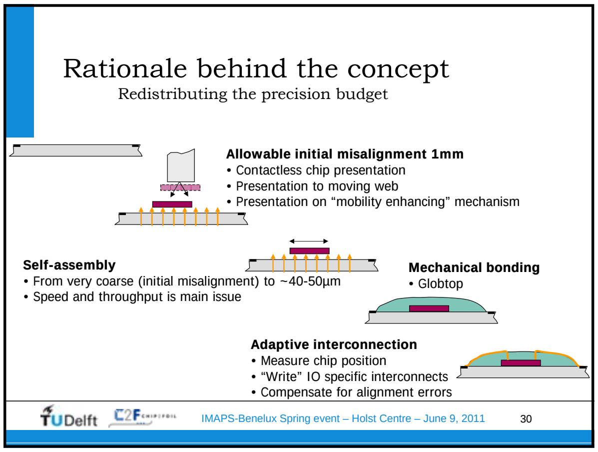
Functions communicative foils

- Focus of Chip2Foil: ultra thin chip integration



- **Self-assembly:** high throughput and low cost, moderate precision

- **Adaptive circuitry:** flexible low-cost interconnection



Rationale behind the concept

Redistributing the precision budget

Allowable initial misalignment 1mm
- Contactless chip presentation
- Presentation to moving web
- Presentation on "mobility enhancing" mechanism

Self-assembly
- From very coarse (initial misalignment) to ~40-50µm
- Speed and throughput is main issue

Mechanical bonding
- Globtop

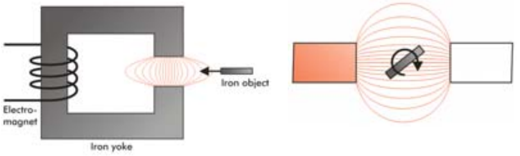
Adaptive interconnection
- Measure chip position
- "Write" IO specific interconnects
- Compensate for alignment errors

Chip2Foil technical work

- UTC assembly:
  - Chip thinning – relationship chip thickness and functionality, chip thickness and process compliance
  - UTC release and presentation
  - **Self-assembly**
  - Mechanical bonding
- Adaptive interconnection
  - Chip position registration
  - Interconnect technology, use of laser machining

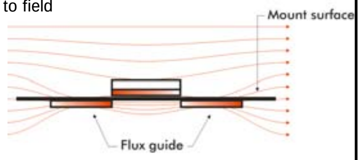
Self-assembly: use of magnetic forces

- Two principles:
  - $F_{magnetic}$ proportional to gradient of magnetic field (square)
  - Shape anisotropy: field lines like to follow path of least resistance



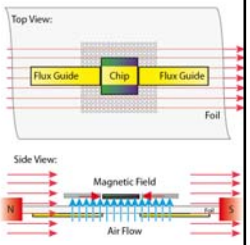
Design

- Magnetic field lines focused by flux guides on substrate
- Flux guides on chip to be aligned make chip susceptible to field



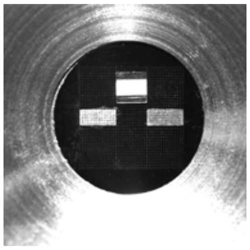
Design

- Magnetic field lines focused by flux guides on substrate
- Flux guides on chip to be aligned make chip susceptible to field
- Enhance chip mobility: air cushion
- Self-assembly on
  - Foil → perforations, sloppy foil
  - Tool → transfer step needed to foil

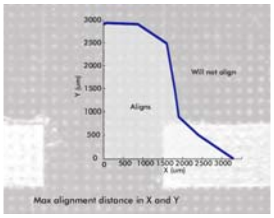


Initial result

- 3mm×3mm parts
- Alignment accuracy 40 µm and 55 µm in x, y directions resp.
- Rotational alignment accuracy of 6°
- Fastest alignment is in 0.4 sec
- Allowable initial misalignment ~ 1 chip size (!)



Initial misalignment range



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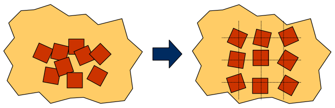
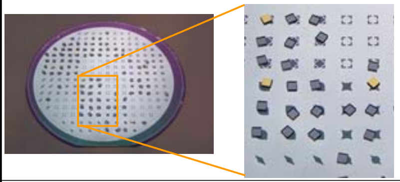
Conclusions and suggestions

- Self-assembly can be promising approach to make breakthrough in assembly process performance
- The field needs industrialisation: demonstrate potential in real and relevant industrial case
- Possible approach:
  - Decompose assembly process in elementary operations
  - Develop single, linkable competences

Example “elementary operations”

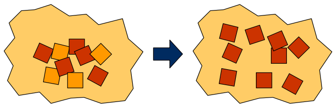
- Spread parts

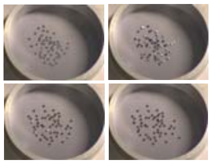


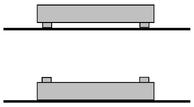


Example “elementary operations”

- Flip parts

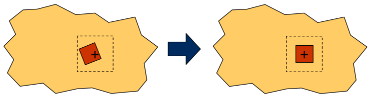






Conclusions and suggestions

- Likely successful operation: self-alignment



- Requires high-throughput low cost presentation approaches
- Teaming up of engineering scientists with innovative industrialists